AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0067] with the following amended paragraph:

[0067] Figure 14 illustrates a block diagram of phase error restart circuit 84, which can be part of the reference accumulator 62. Figure 14 includes a first phase calculator and component 86 and a second phase calculator and component 92. Under normal operation, FCW (frequency control word) is accumulated by adder 86. On each CKR clock, the accumulated FCW passes through multiplexer 88 and is stored in register 90. The output of register 90 is returned to adder 86, which adds the accumulated FCW with the new FCW. The output is the phase reference (PHR), shown in Figures 12b and 12c. However, upon startup (CTL_SRST is high), or end of a mode (OP_ZPR is high at the end of the PVT mode or OA_ZPR is high at the end of the acquisition mode), the output of OR gate 94 controls multiplexer 88 to pass a value equal to FCW+PHV_SMP-PHF (with proper bit alignment). This value will be the new PHR at the end of the PVT mode, the end of the acquisition mode or at startup.